IN THE SPECIFICATION:

Please replace paragraph number **[0003]** with the following replacement paragraph:

[0003] As the integrated circuitry that is carried upon semiconductor substrates becomes ever-smaller and the surface area of such devices becomes ever-larger, the thermal output of such devices increases. Inconsistencies in the properties of the electrically conductive, semiconductive, and non-conductive layers of a semiconductor ~~wafer,~~wafer ~~including~~including, without ~~limitation~~limitation, thickness, sheet resistance, reflectivity, transmissivity, absorptivity, dielectric constant, and various other characteristics of such layers, affect the electrical performance of semiconductor substrates, and therefore contribute, in part, to increased heat output, consequently higher operating temperatures, and other inefficiencies of many state-of-the-art semiconductor substrates.

Please replace paragraph number **[0010]** with the following replacement paragraph:

[0010] However, use of the control system of the '409 patent is somewhat undesirable since it creates and maintains a substantially uniform or "steady state" temperature over the semiconductor ~~wafer,~~wafer which, as explained above, does not facilitate, and actually impedes, reaction rate uniformity. Moreover, due to the ever-increasing size of semiconductor wafers and other substrates, the maintenance of a constant temperature over the surface of such semiconductor wafers may further decrease the uniformity of properties of thin films formed thereon.

Please replace paragraph number **[0017]** with the following replacement paragraph:

[0017] In another embodiment of the inventive process, the reaction chamber temperature is intermittently varied, continually fluctuated or oscillated in order to provide a substantially uniform reaction over the semiconductor substrate while forming a layer thereon. Such fluctuation in the temperature of the reaction chamber may be effected during the ramp-up, the ramp-down, and/or the so-called "steady state" temperature trends. During such fluctuation of the temperature of the reaction chamber, the temperature profile, plotted temperature (y-axis coordinate) over time (x-axis coordinate), may have a saw-tooth (i.e., linear, with small

variations) or a humped configuration. Such variation of the reaction temperature equalizes the reaction rate across the surface of the semiconductor ~~substrate,~~substrate and may be effected by existing fabrication equipment.

Please replace paragraph number **[0033]** with the following replacement paragraph:

[0033] The process of the present invention includes the formation of a material layer, or film, upon an active surface of a semiconductor wafer or other substrate under non-steady state temperature conditions. ~~"Non-steady state",~~"Non-steady state," as used herein, refers to varying, oscillating, continually fluctuating, or summing reaction chamber temperatures with one or more signals of varying frequency, amplitude or phase. Such layers or films may be formed by known deposition or growth techniques or reactions that are modified by employing temperature variation according to the process of the present invention, and using known equipment programmed to effect such temperature variation during the formation of the layer or film. Such deposition and growth techniques include introducing into the reaction chamber matter of a type that promotes the formation of a material layer upon the substrate in proximity to an exposed surface of the substrate.

Please replace paragraph number **[0045]** with the following replacement paragraph:

[0045] For example, when conventional low pressure chemical vapor deposition (LPCVD) techniques, such as the exemplary process that is disclosed in United States Patent 4,395,438 (the ~~"438~~"438 patent"), which issued to Ping-Wang Chiang on July 26, 1983, the disclosure of which is hereby incorporated by reference in its entirety, are employed to form silicon nitride (Si_3N_4) layers on semiconductor wafers, the steady state temperatures within the reaction chamber are typically in the 700° C. to 800° C. range. Silicon nitride deposition in accordance with the process of the present invention includes a controlled ramp-down of the temperature within the reaction chamber from about 780° C. to about 645° C., during which the appropriate, conventionally employed chemical reactants are introduced into the reaction chamber.

Please replace paragraph number **[0046]** with the following replacement paragraph:

[0046] FIGs. 4 and 5 are 49 point contour maps of semiconductor wafers bearing thick (i.e., 1,800Å to 2,000Å) silicon nitride layers. The contour map of FIG. 4 illustrates the thickness of a silicon nitride layer that has been formed upon a semiconductor wafer in a hot wall furnace by conventional steady state temperature deposition techniques. The silicon nitride layer shown in FIG. 4 has a "bowl" or "dish" shaped contour, which is typically caused by reactant gradients over the surface of a semiconductor wafer. As noted previously, when conventional techniques are employed which utilize steady state temperatures throughout the reaction chamber, the reaction rate of the edge region of a semiconductor wafer is higher than the temperature of the center region of the same. Additionally, it is known in the art that thicker layers of some materials form upon the higher temperature regions of a semiconductor wafer than upon the lower temperature regions thereof. Consequently, the use of steady state reaction temperatures throughout a deposition process may result in the formation of a silicon nitride layer having ~~non-uniform~~non-uniform properties due to the generation of reactant gradients thereabove. As illustrated by FIG. 4, the layer is thicker at the edge region of the semiconductor wafer than at its center region. The thickness of the silicon nitride layer varied, from its thinnest measured point (1,808.59Å) to its thickest measured point (1,874.90Å), by about 66Å, which is about 3.6% of the total average layer thickness (1,833.47Å); thus, the standard deviation in layer thickness was about 1.1%.

Please replace paragraph number **[0047]** with the following replacement paragraph:

[0047] In contrast, FIG. 5 is a contour map which depicts the thickness of a silicon nitride layer that has been formed upon a semiconductor wafer in accordance with the second embodiment of the process of the present invention (i.e., during a cool-down phase). The silicon nitride layer of FIG. 5 has a more uniform thickness than that of FIG. 4. The silicon nitride layer varied about 48Å from its thickest measured point (1,859.97Å) to its thinnest measured point (1,811.57Å), which is a variation of about 2.6% from the median thickness (1,836.30Å) of the

layer; thus, the standard deviation of the variation in thickness was only about 0.75%. Moreover, the thickness of the silicon nitride layer depicted in FIG. 5 does not create the bowl shaped contour of FIG. 4, indicating that, when the process of the present invention is employed in order to form a silicon nitride layer upon a semiconductor wafer, the rate at which such a layer is formed on the edge region of the semiconductor wafer is not significantly higher than the rate at which a layer is formed on the center region of the same.

Please replace paragraph number **[0048]** with the following replacement paragraph:

[0048] Similarly, an oxide layer may be formed upon a semiconductor wafer in accordance with the second embodiment of the present invention by techniques that employ tetraethyl-ortho-silicate (TEOS), such as the exemplary process that is disclosed in United States Patent 4,872,947 (the ~~"947"~~"947 patent"), which issued to David N. Wang et al. on October 18, 1989, the disclosure of which is hereby incorporated by reference in its entirety. A semiconductor wafer upon which a layer of TEOS is to be formed is positioned within a reaction chamber while the temperature within the chamber is at an "idle" temperature for conventional TEOS layer formation, about 500° C. The temperature within the reaction chamber is then increased to at least about the temperature at which TEOS layer formation by conventional processes occurs, about 600° C. to about 625° C., which is referred to as a first temperature. A controlled ramp-down of the temperature within the reaction chamber to a second, or termination, temperature is then effected. During the controlled ramp-down, the appropriate, conventionally employed chemical reactants are introduced into the reaction chamber, wherein a TEOS layer forms on a surface of the semiconductor wafer. After a TEOS layer of the desired thickness has been formed, the temperature within the reaction chamber may be reduced to "idle" and the semiconductor wafer removed therefrom.

Please replace paragraph number **[0053]** with the following replacement paragraph:

[0053] In another embodiment of the layer formation process of the present invention, the temperature within the reaction chamber may be oscillated, fluctuated, or intermittently varied during at least a portion of any of the heat-up, substantially steady state, or cool-down

phases, or any combination thereof. Such intermittent variation of the temperature generates and maintains a substantially uniform temperature over the surface of a semiconductor wafer. Temperature uniformity over the surface of a semiconductor wafer is desirable for layer forming processes including, without limitation, dopant diffusion, alloying or any other diffusion-limited process, and the formation of multiple layers having different coefficients of expansion. Additionally, the generation of substantially uniform temperature over a semiconductor wafer may reduce or eliminate stresses that may result in the formation of lattice defects, such as point, line (~~e.g.~~e.g., slip, straight dislocations, dislocation loops, etc.), area, volume, or other thin film defects.

Please replace paragraph number **[0054]** with the following replacement paragraph:

[0054] During the heat-up phase, the process of the present invention may include an oscillating increase in the temperature within the reaction chamber. As the temperature within the reaction chamber is ramped up during the heat-up phase, each increase in reactor temperature is followed by a temperature decrease. As illustrated by FIG. 7, a linear graph of such a heat-up phase, wherein temperature is plotted over time, includes fluctuations in temperature which impart the graph with a saw tooth, or a ~~zig-zag,~~zig-zag configuration. Other oscillating heat-up patterns are also within the scope of the present invention, as are less predictable variations in the reactor temperature during the heat-up or anneal phases. The amount of temperature variation between the high and low points of each zig-zag and the durations of each temperature increase and subsequent temperature decrease are optimized in order to provide uniform temperatures across the semiconductor wafer at all times during the formation of a layer or film thereon. This embodiment of the present invention facilitates a uniform cross-wafer temperature during either of the heat up or cool down phases. Although the graph of FIG. 7 represents each fluctuation as an increase in temperature followed by a smaller decrease in temperature, temperature increases that are followed by no change (as illustrated by FIG. 7a) in temperature for a period of time or by lower rate temperature increases are also within the scope of the present invention.

Please replace paragraph number **[0063]** with the following replacement paragraph:

[0063] An exemplary material layer formation system 16, which is depicted in FIG. 12, includes a reaction chamber 20 with a heating element 22 therein. System 16 may also include a temperature sensor 17, or feedback system, of a type known in the art. Temperature sensor 17 is at least partially located within reaction chamber 20 so as to facilitate measurement of the temperature within reaction chamber 20 or of various portions of a semiconductor wafer 24 or other substrate within reaction chamber 20. Semiconductor wafers 24a, 24b and 24c upon which a material layer is to be formed are positioned on a platen 23 in reaction chamber 20. Platen 23 may be rotated by way of a rotator 25. Reaction chamber 20 is heated to a desired temperature by inputting power into heating element 22. As the temperature within reaction chamber 20 increases, the temperature of each of semiconductor wafers 24a, 24b and 24c increases. ~~A~~An edge heater 21 may also be positioned within reaction chamber 20 so as to increase the temperature of at least an edge of one or more semiconductor wafers 24 or other substrates located in reaction chamber 20. When the temperature of reaction chamber 20 reaches a first, or initial anneal, temperature, matter 26 of a type that will promote the formation of a material layer upon each of semiconductor wafers 24a, 24b and 24c is introduced into reaction chamber 20 through an inlet 28. Preferably, the introduction of matter 26 into reaction chamber 20 is continued until the reaction chamber reaches a second, or terminal anneal, temperature.

Please replace paragraph number **[0064]** with the following replacement paragraph:

[0064] Preferably, in order to form uniform layers upon semiconductor wafers, the frequency and amount of temperature variation of the process of the present invention are optimized for the type of layer formed, the desired layer properties, and the equipment with which the layer is formed. Similarly, depending upon the initial growth pattern of a formed layer, the amount and rate of temperature variation may be altered or optimized in order to enhance uniformity in the properties of the layer. Moreover, repetition of the process, as well as oscillating the temperature within the reaction ~~chamber~~chamber, may be employed to form substantially uniform layers upon the surface of a semiconductor wafer.

Please replace paragraph number **[0067]** with the following replacement paragraph:

[0067] The process of the present invention may be employed by various types of existing ~~systems,~~systems ~~including~~including, without ~~limitation~~limitation, hot and cold wall, single wafer and multiple wafer, vertical and horizontal, plasma-enhanced systems with or without wafer rotation, atmospheric pressure, high pressure and low pressure reactors. The inventive process may also be used with systems which are typically incapable of maintaining uniform temperatures throughout their reaction chambers, and ~~were~~were, ~~therefore~~therefore, previously considered undesirable for forming certain types of layers. Advantageously, substantially uniform layers may be formed in existing semiconductor substrate fabrication equipment without requiring expensive modifications thereto or the replacement thereof.